ESE355: VLSI System Design

Instructor: Dr. Alex Doboli, **adoboli@ece.sunysb.edu**
TA: TBA

Class schedule:
Lab:
Office hours: Monday and Wed 1-3pm, Light Engineering Bldg. 261

Catalog Description: Introduces techniques and tools for scalable VLSI design and analysis. Emphasis is on physical design and on performance analysis. Includes extensive lab experiments and hand-on usage of CAD tools.

Course Designation: Elective for EE and CE

Text Book: Jan Rabaey, A. Chandrakasan, B. Nikolic, "Digital Integrated Circuits: A Design Perspective", Prentice Hall, 2003.

Reference: Neil Weste, D. Harris, "CMOS VLSI Design", Third Edition, 2005

Prerequisites: ESE218
Corequisite: none

Goals: The course introduces techniques and tools for scalable VLSI design and analysis. The emphasis is on physical design and on performance analysis. The course includes extensive lab experiments, a mini project and hands-on usage of CAD tools.

Objectives: Upon completion of this course, students are able to develop, layout and simulate fabricatable designs of VLSI building blocks, such as registers, arithmetic units, finite state machines, and medium-scale VLSI chips. Students are knowledgeable to design digital circuits optimized for timing and area constraints.

Topics Covered:

Week 1.	**Introduction to design of VLSI systems and circuits. The MOSFET Transistor**. Static behavior. Dynamic behavior. Secondary effects. SPICE models for the MOS transistor. Small-signal models.
Week 2.	**The CMOS Inverter**. Static behavior.
Week 3.	**The CMOS Inverter**. Dynamic behavior. Propagation delay. Power consumption.
Week 4.	**Combinational Logic Gates**. Complementary CMOS design
Week 5.	**Combinational Logic Gates**. Complementary CMOS design. Layout techniques for complex gates. Bit-slice design. Pipelining.
Week 6.	**Combinational Logic Gates**. Dynamic CMOS. Principles. Performance. Cascading.

Week 7.	**Combinational Logic Gates**. Dynamic CMOS. Principles. Performance. Cascading.
Week 8.	**Design of Sequential Circuits.** flip-flops. master-slave ff. CMOS static flip-flops. Implementation with PLA structures. Application.
Week 9.	**Design of Sequential Circuits.** flip-flops. master-slave ff. CMOS static flip-flops. Implementation with PLA structures. Application.
Week 10.	**Design of Sequential Circuits.** Dynamic sequential circuits. Pseudo static latch. Dynamic two-phase flip flop. C2MOS latch. NORA-CMOS structure.
Week 11.	**Design for Testability.**
Week 12.	**Interconnect.** Crosstalk. Resistive parasitic. Inductive parasitic. Packaging technology.
Week 13.	**Timing Issues in Digital Circuits.** Clock Skew. Single & two-phase clocking. countering of clock skew problems.

Class/laboratory Schedule: 3 lecture hours and 3 laboratory hours per week.

Grading: Final Grade = *Homework*$_1$ * 0.05 + *Homework*$_2$ * 0.1 + *Homework*$_3$ * 0.1 + *Homework*$_4$ * 0.1 + *Mid-term* * 0.2 + *Final* * 0.2 + *Mini Project* * 0.2 + *Course portfolio* * 0.05

Exam schedule:

Midterm: Wednesday - Week 8, 10:40-11:35am.
Final exam: Exam week

Homework schedule:

	Points	Start date	Due date
Homework1	5	Mo Week 2	We Week 3
Homework 2	10	We Week 3	Fr Week 4
Homework 3	10	Fr Week 4	We Week 6
Homework 4	10	We Week 6	Mo Week 8